

## DESIGNING CODEC TO IMPROVE CHIP PERFORMANCE FOR LOW-POWERED UNRELIABLE COMPONENTS

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### ABSTRACT

This research introduces a new innovation in achip design. So far, chip fabrication technology has reached the nanometer scale where the issue of unreliable components becomes crucial wherean error on the chip level can damage the overall performance of a system. This research seek to test methods of designing and architecturing a new codec that can achieve Shannon Limit without reducing the chip performance. In so doing, Moore's Law will still apply. The Information Theory by Shannon, will be implemented at the chip level. It was assumed that the way of communication was more or less equal in a physical level, so the Low Density Parity Code (LDPC) with some modifications can be expected to give a result. This research is done in four gradual stages in order to understand, develop, design and simulate, and implement the methods of research on an actual device. The result could have a huge impact in the evolution of information technology and computer infrastructure. While the focus of this research is the technology of Complementary Metal-Oxide-Semiconductor (CMOS), it certainly can be implemented in other technologies.

**Keywords:** chip, codec, CMOS, information theory, LDPC, Shannon

This research will focus on finding an innovation way to design a chip. This is relevant because the improvement in nanotechnology chip

fabrication method has brought benefits in terms of size reduction and low power consumption. The reduction in size causes an unreliable issue and bring up an error. At the chip level, even one bit error could affect the entire system. As an example, in the Toyota Case (Yoshida, 2013), Yoshida reported a sudden acceleration in a Toyota Camry caused a death. Oklahoma County jury ruled that Toyota was liable for the crash as atestimony from an embedded system expert pointed to a bug in the system that caused an unintended acceleration. Even though this case was not directly related to chip fabrication, it gave an insight into the severe consequence that could be caused by a system damage.

This research seeks to find and test a new method in chip and codec design that fits with Shannon limit without reducing chip performance significantly and continues, Moore's law. It will bring Shannon's Information Theory to a new low level for chip production. The chip is built using a Very Large Scale Integration (VLSI) system that incorporated low-energy consumption. But it is sometimes inherently unreliable in nano-scale (S. Ghosh, 2010) due to the unreliable logic gates with transient failures. The reliability could be resolved by employing a variety of methods such as Low Density Parity Check (LDPC) codes (B. Vasic, 2007), Gallager-B algorithm (F. Leduc-Primeau, 2012), and also min-sum algorithm (A. Balatsoukas-Stimming, 2014).

## LITERATURE REVIEW

Bit flipping algorithms are decoding algorithms for LDPC codes and the fastest and least complex on the binary symmetric channel (BSC). There are several bit flipping algorithms, such as parallel and serial bit flipping. The parallel bit flipping algorithm can asymptotically correct a linear number of errors for almost all codes

with left degree  $\geq 5$  (V. Zyablov, 1976). Regular codes with left degree equal to 4 are also capable of correcting a linear number of errors under the parallel bit flipping algorithm (Burshtein, 2008). The serial bit flipping algorithm can correct a linear number of errors in underlying Tanner graph with a good expander (M. Sipser, 1996).

Empirical evaluation of the performance of LDPC codes using a Gallager-B decoder built from unreliable components showed that the obtained numerical results could be applied for designing memory architecture (O. Al Rasheed S. S., 2014). The researchers examined the influence of different code parameters, decoder structures and fault model parameters. These parameters were observed in the overall system performance, so the researchers could gain insights into the relative importance of failures in different logic gates and their relationships with parameters such as code length and number of iterations. The min-sum algorithm was also investigated. The asymptotic and finite-length behavior of the noisy min-sum decoder produced a refined probabilistic error model (C. L. K. Ngassa, 2014). Since an inappropriate choice of the channel scale factor can lead to an unconventional behavior, a correction capacity could be increased with respect to the noiseless decoder when the noise is introduced by the device.

## **THEORETICAL FRAMEWORK**

### **Information Theory**

The Information theory was introduced by C. E. Shannon in 1948 (Shannon, 1948) in Bell Telephone Laboratories, as a communication system for telephony. Weaver expanded this concept by implementing it to all communications (C. E. Shannon, 1963). With the current communication and computation technology



advancement, the fields of communication and computation have converged and it is common to see communication forms using telephony line, computer network, cellular network, and so on.. However these forms are unimportant as communication can take place inside a chip or an electronic circuit. While this makes communication much simpler, the accuracy becomes of paramount importance. This calls for a refinement of the theory, such as adding a feedback where a correction would be triggered if errors were raised. In this way, observer would be function as a codec which had an auto-correction mode. This correction mode should use a brief and accurate method so the overall system should not be burdened, like the LDPC (Yeung, 2008). This is massively used in channel coding and with its low parity feature, it could perform as high as Shannon's limit.

### Hamming Code

Hamming code is a linear block code (LBC) in a size of  $(n, k)$  with the length of bit check vector greater than 3 ( $q \geq 3$ ). The  $n$  value depends on  $q$ , which is described by formula (1).

$$n = 2^q - 1 \quad (1)$$

Hence, the value of  $k$  depends on  $n$  and  $q$ . This will be described in formula (2).

$$k = n - q \quad (2)$$

With these two variables, we can calculate code rate ( $R_c$ ). This variable will be described in formula (3).

$$R_c = \frac{k}{n} = 1 \quad (3)$$

From formula (3), it could be concluded that  $R_c \approx 1$  if  $q \gg 1$ , so the minimum distance for hamming code will be always 3 (Moon, 2005). This minimum distance would effect the maximum of errors that

could handle by the system. With the minimum distance of 3, this hamming code can be used to correct one or two errors in one time.

## LINEAR BLOCK CODE

### Generator Matrix

The linear code is a vector space where each code word is a vector. The group of these code words with the length of  $n$  is called linear block code (LBC). The only rule is the group should be a subspace of a vector space of  $n$ -tuple. Matrix representation of a code is an ideal way to describe the code itself. A linear code with a size of  $(n, k)$  is defined by generator matrix  $G$  with the dimension of  $k \times n$ . Each line of  $G$  matrix is  $n$ -tuple, and each column of  $G$  matrix is  $k$ -tuple. This could be concluded that  $c$  could be constructed by using formula (4).

$$c = d_0g_0 + d_1g_1 + \dots + d_{k-1}g_{k-1} \quad (4)$$

With variable  $d$  is data. The size of  $d$  is  $d_i$  ( $0 < i < k-1$ ) and  $g$  is subspace of  $G$  which is  $g_i$  ( $0 < i < k-1$ ). The encoding procedure could be represented by formula (5).

$$C = d.G \quad (5)$$

With  $G$  is defined as  $G = [P_{k \times (n-k)} \mid I_k]$ .

### Parity-Check Matrix

The matrix  $H$  is parity-check matrix for matrix generator,  $G$  with a size of  $(n-k) \times n$ . For the matrix  $G$  that is described in the above subsection, matrix  $H$  is formulated as specified in formula (6).

$$H = [I_{n-k} \mid P_{(n-k) \times k}^T] \quad (6)$$

With  $P^T$  is transpose matrix for sub-matrix  $P$ .

### Syndrome

Assumed that  $c = (c_0, c_1, \dots, c_{n-1})$  is a code word that is transmitted and  $r = (r_0, r_1, \dots, r_{n-1})$  is a word that is received from the demodulator output. This  $r$  variable could be equal or different from  $c$  variable, depending on the noise in the channel. If  $r \neq c$ , this could be corrected by equation  $r = c + e$ , with  $e = r - c = (e_0, e_1, \dots, e_{n-1})$  where  $e$  is the error. After receiving  $r$ , the decoder will start to count the syndrome. This syndrome can be used to locate errors and attempts to correct them. The syndrome is noted by a variable  $s$  as stated in formula (7).

$$s = r \cdot H^T = (s_0, s_1, \dots, s_{n-k-1}) \quad (7)$$

with  $c \cdot H^T = 0$ , the formula (7) could be stated in simple form as in formula (8).

$$s = e \cdot H^T \quad (8)$$

This formula shows the relation between syndrome and error. So, if  $s = 0$ , it could be concluded that  $e = 0$  or there is no error. If  $s \neq 0$ , then  $r \neq c$ . This means there are errors.

### METHODOLOGY

In information theory, an error correction code which is tolerable to error is important. Shannon showed that it is possible to do a reliable communication in an unreliable channel.

LBC is one of the methods that enable reliable communication to be done in an unreliable channel. As it is suited to the LDPC criteria, research is carried out to implement it in the internal communication in an integrated circuit (IC). Implementation of LDPC is cheaper than other LBC codes with the same performance. Also, with the LDPC code, Shannon's limit is still achievable, which is the minimum for reliable communication in noisy channel. This research intends to

examine the features of LDPC, so the code could be understandable and redirected to an implementation. This research will also identify LBC code that is suitable for LDPC and the way to implement it.

As a first step, this research will evaluate a number of LBC codes that are suitable to be treated as LDPC. These codes can be simulated by using Ms. Excel. With Ms. Excel, this code will be implemented as logic calculation. Figure 1 shows an example.

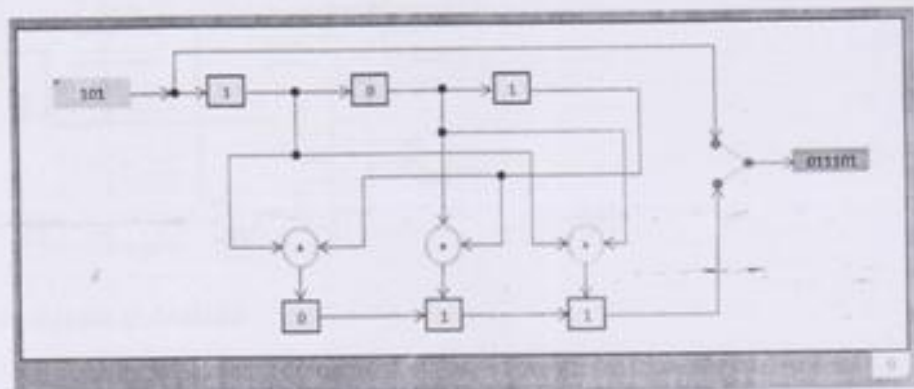


Figure 1. Encoder Simulation in Ms. Excel

With this diagram, the computation process is traceable - the *code*, *codeword*, the kind of computation, the *code word*, the *received code*, the *syndrome*, and also the result with or without errors. This simple diagram and implementation will give an indication of the system performance.



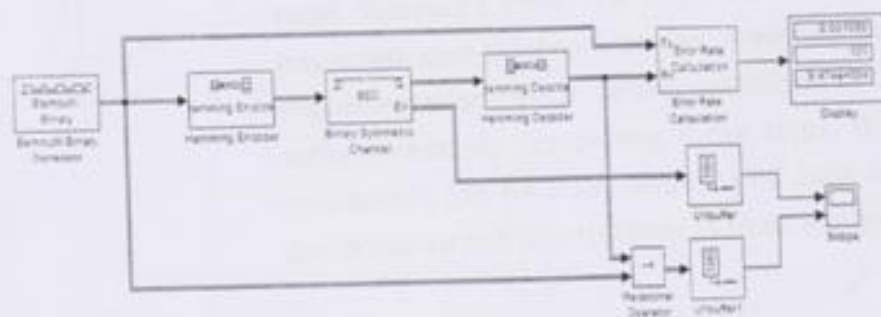


Figure 2. Simulation in Matlab

After the evaluation, the next step is do a simulation with Matlab. In this simulation, a number of channel is implemented to see the overall system performance. The outputs from this simulation are an error rate, number of errors and the comparison between data. Figure 2 shows a sample of this simulation using a binary symmetric channel (BSC).

The third step is a real implementation. A number of candidates of LDPC codes is implemented in microcontroller modules. These modules are set up in a way that they are functioning as a receiver and a transmitter so that the LDPC codes could be implemented directly in the hardware. Data transmission with or without errors could be applied directly. The results are shown immediately.

Finally, all other LDPC codes performance are recorded and discussed

## RESULT

**RESULT**

This research demonstrates that a new codec with implementation in hardware could be developed. It will show that LDPC is the right



choice in error detection and correction method in low level data transmission.

### DISCUSSION

The research detailed steps taken to search for LDPC code that can meet Shannon's limit. The steps ensured that LDPC code could be inspected step-by-step from its mathematical foundation until its implementation in a microcontroller. Each step has its own achievement. By completing these steps, this research will enable conclusions can be made about LDPC code and show its complexity, performance and also its chances to be implemented.

### CONCLUSION

LDPC is a method which has been well developed, but there is still a possibility for research in areas like the type of generator matrix, the performance in a variety of channels, and a more efficient hardware implementation. There is a need to find out a more low cost hardware implementation for LDPC code since in commercial usage, a low cost implementation is important.

This research looks at LBC as a solution for LDPC code. By understanding the implementation of the LDPC code as a codec in hardware, information can be obtained regarding its implementation cost, performance and also its complexity. While the production technology is not mature, this research can help the chip to perform better. Like in the beginning of microprocessor technology, a kind of codec was needed to increase the hardware performance. But when the technology mature, this kind of codec was discontinued.

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